AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Claim 1 (Currently amended): A serializer/deserializer communications system, comprising:

a transmitter, the transmitter coupled to receive N parallel bits of data and transmit the N parallel bits of data into K frequency separated channels on a single conducting differential transmission medium, where N and K are integers each greater than one, the N parallel bits being transmitted into the K frequency separated channels of the serializer/deserializer system synchronously; and

a receiver coupled to receive a sum signal that includes signals from each of the K frequency separated channels from the single conducting differential transmission medium and recover the N parallel bits of data,

wherein the receiver includes K demodulators, each of the K demodulators receiving signals on one of the K frequency separated channels, at least one of the K demodulators including

an analog down converter that converts the signal corresponding to that channel associated with the at least one of the demodulators to a base-band signal in a single step;

an analog-to-digital converter coupled to receive the base-band signal from the analog down converter and generate a digitized base-band signal;

an equalizer circuit coupled to receive the digitized base-band signal and create an equalized symbol; and

a decoder that synchronously retrieves~~receives~~ the equalized symbol and retrieves bits associated with the at least one of the K demodulators.

Claim 2 (Previously presented): The system of Claim 1, wherein the transmitter comprises

a bit allocation circuit that receives the N parallel bits of data and creates K subsets of data bits;

K modulators, wherein each of the K modulators encodes one of the K subsets of the N parallel bits of data and creates an output signal modulated at a carrier frequency associated with one of the K frequency separated channels; and

an adder that receives the output signal from each of the K modulators and generates a transmit sum signal for transmission on the single conducting differential transmission medium.

Claim 3 (Previously presented): The system of Claim 2, wherein at least one of the K modulators includes

a data encoder that receives the one of the K subsets of the N parallel bits of data associated with the at least one of the K modulators and outputs an encoded signal;

a symbol mapper coupled to receive the encoded signal and output a symbol; and

an analog up-converter coupled to receive symbols from the symbol mapper and generate the output signal,

wherein the analog up-converter outputs data at the carrier frequency of one of the K frequency separate channels that corresponds with the at least one of the K modulators.

Claim 4 (Previously presented): The system of Claim 3, further including a digital-to-analog converter coupled between the symbol mapper and the analog up-converter.

Claim 5 (Original): The system of Claim 3, wherein the data encoder is a trellis encoder.

Claim 6 (Previously presented): The system of Claim 3, wherein the symbol mapper is a QAM symbol mapper which maps the encoded output signal into a complex symbol that includes an in-phase signal and a quadrature signal.

Claim 7 (Original): The system of Claim 4, further including a digital filter coupled between the symbol mapper and the digital-to-analog converter.

Claim 8 (Previously presented): The system of Claim 4, further including a low-pass analog filter coupled between the digital-to-analog converter and the analog up-converter.

Claim 9 (Previously presented): The system of Claim 6, wherein the analog up-converter generates a first signal by multiplying the in-phase signal of the complex symbol by a sine function of the carrier frequency, generates a second signal by multiplying the out-of-phase signal of the complex symbol by a cosine function of the carrier frequency, and summing the first signal with the second signal to generate the output signal.

Claim 10 (Previously presented): The system of Claim 1, wherein the single conducting differential transmission medium is a copper backplane and the transmitter includes a differential output driver.

Claim 11 (Previously presented): The system of Claim 1, wherein the single conducting differential transmission medium includes an FR4 copper trace and the transmitter includes a differential output driver.

Claim 12 (Canceled).

Claim 13 (Previously presented): The system of Claim 2, wherein a subset of bits at a lower carrier frequency contains more bits than a subset of bits associated with a higher carrier frequency.

Claim 14 (Original): The system of Claim 2, wherein each of the K subsets of data bits includes the same number of data bits.

Claim 15 (Previously presented): The system of Claim 2, wherein the receiver comprises:

a bit parsing circuit that receives each of the K subsets of data bits from the K demodulators and reconstructs the N data bits transmitted by the transmitter.

Claim 16 (Previously presented): The system of Claim 15, wherein the receiver further includes an input buffer coupled between the K demodulators and the single conducting differential transmission medium.

Claim 17 (Previously presented): The system of Claim 16, wherein the input buffer receives a differential receive sum signal that is input to the analog down converter.

Claims 18-20 (Canceled).

Claim 21 (Previously presented): The system of Claim 1, further including an anti-aliasing filter coupled between the analog down-converter and the analog-to-digital converter.

Claim 22 (Previously presented): The system of claim 1, further including a variable gain amplifier coupled between the down converter and the analog-to-digital converter, the variable gain amplifier being controlled by an automatic gain circuit.

Claim 23 (Previously presented): The system of Claim 1, wherein the digitized base-band signal includes an in-phase signal and a quadrature signal and the analog down-converter multiplies the sum signal by a cosine function to retrieve the in-phase signal and by a sine function to retrieve the quadrature signal.

Claim 24 (Previously presented): The system of Claim 1 further including an adaptively controlled digital filter coupled between the digital-to-analog converter and the equalizer.

Claim 25 (Previously presented): The system of Claim 24, further including a phase-rotator coupled between the adaptively controlled filter and the equalizer.

Claim 26 (Previously presented): The system of Claim 1, wherein the equalizer parameters are adaptively chosen.

Claim 27 (Currently amended): A method of communicating between components over a single conducting differential transmission medium, comprising:

~~separating~~ synchronously serializing N bits into K subsets of bits;

encoding each of the K subsets of bits to form encoded subsets of bits;

mapping each of the K encoded subsets of bits onto a symbol set to generate K symbols representing each of the K subsets of bits;

converting each of the K symbols to K analog signals;

up-converting each of the K analog signals in a single analog up-conversion step to form K up-converted signals corresponding with a set of K carrier frequencies;

summing the K up-converted signals representing each of the K subsets of bits to generate a transmit sum signal;

coupling the transmit sum signal to the single conducting differential transmission medium;

receiving a receive sum signal from the single conducting differential transmission medium, the receive sum signal being the transmit sum signal after transmission through the single conducting differential transmission medium;

down-converting the received sum signal in a single analog down-conversion step for each of the K carrier frequencies into a set of K signals at a base band frequency;

digitizing each of the set of K signals to form K digitized signals;

equalizing each of the K digitized signals to receive K equalized symbols; and

decoding each of the K synchronously equalized symbols to reconstruct the K subsets of bits; and

parsing K subsets of bits into N deserialized bits.

Claim 28 (Original): The method of Claim 27, wherein symbols transmitted at lower carrier frequencies represent fewer bits than symbols transmitted at higher carrier frequencies.

Claim 29 (Original): The method of Claim 27, wherein encoding each of the K subsets of bits includes encoding at least one of the K subsets of bits with a trellis encoder.

Claim 30 (Original): The method of Claim 27, wherein mapping each of the encoded subsets of bits includes QAM mapping.

Claim 31 (Canceled).

Claim 32 (Previously presented): The method of Claim 27, further providing digital filtering prior to converting the K symbols to K analog signals.

Claim 33 (Previously presented): The method of Claim 27, further providing analog filtering of each of the K analog signals.

Claim 34 (Canceled).

Claim 35 (Previously presented): The method of Claim 27 wherein receiving the receive sum signal includes receiving a differential signal from a copper backplane.

Claim 36-37 (Canceled).

Claim 38 (Previously presented): The method of Claim 27 further including providing automatic gain conversion for each of the set of K signals prior to digitizing each of the set of K signals.

Claim 39 (Canceled).

Claim 40 (Previously presented): The method of Claim 27, further including anti-aliasing filtering prior to analog-to-digital conversion.

Claim 41 (Previously presented): The method of Claim 27 further including providing adaptively controlled filtering for timing recovery.

Claim 42 (Previously presented): The method of Claim 27 wherein the K equalized symbols are complex and further providing adaptively controlled phase rotation.

Claim 43 (Previously presented): The method of Claim 27 wherein decoding the equalized symbols includes trellis decoding and QAM decoding.

Claim 44 (Currently amended): A system for communication between components, comprising:

means for synchronously serializing ~~allocating~~ N bits of input data into K subsets;

means for encoding each of the K subsets;

means for transmitting each of the K subsets into one of K channels on a single conducting differential transmission medium, wherein the means for transmitting includes an up-converter that up-converts in a single analog step for each of the K channels and sums the resulting upconverted signal into a summed signal for transmission over the single conducting differential transmission medium;

means for receiving data from the K channels, the means for receiving including an analog down converter and an analog to digital converter coupled to the analog down converter;

means for correcting the data for intersymbol interference coupled to the means for receiving;

means for synchronously retrieving the K subsets; and

means for ~~retrieving~~ deserializing the N data bits from the K subsets.

Claim 45 (Canceled).

Claim 46 (Currently amended): A transceiver chip for a serializer/deserializer system, comprising:

a transmitter portion, the transmitter portion coupled to receive N parallel bits of data and transmit the N parallel bits of data into a first set of K frequency separated channels on a first single conducting differential transmission medium, the N parallel bits being transmitted into the K frequency separated channels of the serializer/deserializer system synchronously where N and K are integers each greater than one; and

a receiver portion coupled to receive data from a second set of K frequency separated channels from a second single conducting differential transmission medium and recover a second N parallel bits of data, wherein the receiver portion includes,

K demodulators, each of the K demodulators coupled to receive a signal from the second single conducting differential transmission medium, the signal being a transmit sum signal transmitted through the second single conducting differential transmission medium, and retrieving one of the K subsets of data bits and a bit parsing circuit that receives each of the K subsets of data bits from the K demodulators and reconstructs the N data bits transmitted by the transmitter, and

wherein at least one of the K demodulators comprises

an analog down-conversion circuit that receives the signal from the second single conducting differential transmission medium and generates a symbol by converting the signal at the carrier frequency appropriate for the one of the K demodulators,

an analog to digital converter coupled to digitize the symbol from the analog down conversion circuit,

an equalizer circuit coupled to receive the digitized symbol from the analog to digital converter and create an equalized symbol; and

a decoder which receives the equalized symbol and synchronously retrieves the one of the K subsets of bits associated with the at least one of the K demodulators.

Claim 47 (Original): The chip of Claim 46, wherein the first set of K frequency separated channels have substantially identical carrier frequencies with the second set of K frequency separated channels.

Claim 48 (Previously presented): The chip of Claim 46, wherein the transmitter comprises:

a bit allocation circuit that receives the N parallel bits of data and creates K subsets of data bits; and

K modulators, wherein each of the K modulators encodes one of the K subsets of the N parallel bits of data and creates an output signal modulated at a carrier frequency associated with one of the first set of K frequency separated channels; and

an adder that receives the output signal from each of the K modulators and generates a transmit sum signal for transmission on the first single conducting differential transmission medium.

Claim 49 (Previously presented): The chip of Claim 48, wherein at least one of the K modulators includes

a data encoder that receives the one of the K subsets of the N parallel bits of data associated with the at least one of the K modulators and outputs an encoded signal;

a symbol mapper coupled to receive the encoded signal and output a symbol;

a digital to analog converter that digitizes the symbols from the symbol mapper; and

an analog up-converter coupled to receive the digitized symbols from the digital to analog converter and generate the output signal,

wherein the up-converter outputs data at the carrier frequency of one of the K frequency separate channels that corresponds with the at least one of the K modulators.

Claim 50 (Original): The chip of Claim 49, wherein the encoder is a trellis encoder and the symbol mapper is a QAM symbol mapper.

Claims 51-52 (Canceled).